Practitioner's Docket No.: 989_001DIV6 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

James E. Moon et al.

Ser. No.: Not Assigned

Filed: Concurrently Herewith

Parent Appln. Information:

Serial No. 09/334,408

Filed: June 16, 1999

For: METHOD FOR FABRICATING LC DEVICE USING LATENT MASKING AND DELAYED LOCOS TECHNIQUES

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 addressed to the **Box Patent Application, Assistant Commissioner for Patents, Washington D.C. 20231** on November 2, 2001.

Cheryl M. Nichols

Cheryl M. Nichols

Box Divisional Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows before examination thereof.:

In the Claims:

Please cancel claims 1-19 and 23, amend claim 20, and add new claims 24-29 as follows:

20. (Amended) A method for fabricating a liquid chromatography microelectromechanical device, comprising the steps of:

a) providing a silicon substrate having an introduction surface on an introduction side of said substrate and an opposing separation surface on a separation side of said substrate;

b) forming first and second silicon oxide layers on said introduction and separation surfaces of said substrate, respectively;

c) doping a portion of said introduction surface through said first silicon oxide layer with a dopant of a same conductivity type as a conductivity type of said substrate;

d) forming a silicon nitride film on said first silicon oxide layer;

e) patterning and etching said silicon nitride film to form at least one silicon nitride contact area on said first silicon oxide layer;

f) oxidizing said substrate, after step (e), to increase said first and second silicon oxide layers;

g) coating a first photoresist layer on said introduction side;

h) defining a first pattern on said first photoresist layer, said first pattern consisting of an introduction channel and an introduction-side exit channel;

i) transferring said first pattern onto said first silicon oxide layer;

j) etching said first pattern into said silicon substrate;

k) removing said first photoresist layer;

l) coating a second photoresist layer on said separation side;

m) defining and transferring a second pattern onto said second silicon oxide layer, said second pattern including a separation channel, a separation channel terminus, and a plurality of separation posts;

n) removing said second photoresist layer;

o) coating a third photoresist layer on said separation side;

p) defining and transferring a third pattern consisting of a fluid reservoir and a separation-side exit channel onto said second silicon oxide layer when said second pattern does not include said fluid reservoir, such that said reservoir is substantially aligned with said introduction channel and said separation-side exit channel is substantially aligned with said introduction-side exit channel; otherwise, defining said third pattern onto said separation surface when said fluid reservoir is also included in said second pattern, such that said reservoir is substantially aligned with said introduction channel and said separation-side exit channel is substantially aligned with said introduction-side exit channel;

q) etching said third pattern into said silicon substrate so that said reservoir connects with said introduction channel and said separation-side exit channel connects with said introduction-side exit channel;

r) removing said third photoresist layer;

s) etching said second pattern into said silicon substrate;

t) forming, after step (s), an isolation layer on all silicon surfaces of said silicon substrate;

u) attaching, after step (t), a cover substrate to said separation surface of said silicon substrate;

v) removing, after step (u), said silicon nitride from said at least one silicon

nitride contact area and removing any of said first silicon oxide layer beneath said at least one silicon nitride contact area, thereby forming at least one contact area on said first surface; and

w) depositing a metal on said at least one contact area.

24. (New) A method according to claim 20, wherein said etching in at least one of steps (e), (j), (q), and (s) is performed by dry etching.

25. (New) A method according to claim 20, wherein said step of removing said silicon nitride is performed by wet etching in hot phosphoric acid.

26. (New) A method according to claim 20, wherein said step of removing said silicon nitride and said pad oxide is performed as an unmasked etch by reactive ion etching.

27. (New) A method according to claim 20, further comprising shadow masking, before step (v), said at least one silicon nitride contact area and wherein said step of removing said silicon oxide and said oxide is performed by reactive ion etching.

28. (New) A method according to claim 20, wherein step (c) is performed before step (d).

29. (New) A method according to claim 20, wherein step (c) is performed after step (v) and before step (w).

REMARKS

Claims 20-22 and 24-29 are pending herein. Claims 1-19 and 23 are cancelled, claim 20 is amended, and new claims 24-29 are added.

The following is provided to assist the Examiner in his examination of the claims. Three etching techniques are used to create microelectromechanical (MEMS) and/or microfluidic devices. These techniques can be used singly or in various combinations with each other. These techniques are referred to in the description as Latent Masking, SMILE, and delayed LOCOS.

Latent Masking defines a mask in a persistent material like silicon oxide that is held abeyant after definition while intervening processing operations are performed. The intervening steps do not disturb nor are disturbed by the mask. After the intervening steps are performed, the latent oxide pattern is then used to mask an etch. Latent Masking is presented in claims 1-3. These claims are cancelled in this application.

SMILE, which is an acronym based on "simultaneous multi-level etching", provides a process sequence wherein a first pattern may be given an advanced start relative to a second pattern in etching into an underlying material, such that the first pattern may be etched deeper, shallower, or to the same depth as the second pattern. This process allows etching two different patterns into a substrate such that the final depth of the two patterns is independently controlled. SMILE is presented in claim 4. A variant of SMILE is presented in claim 5 in which the SMILE technique is applied to three patterns instead of only two patterns. These claims are cancelled in this application.

Delayed LOCOS provides a means of defining a contact hole pattern at an early stage of a process, then using the defined pattern at a later stage to open the contact holes. This is an alternative to the well known process of LOCOS (local oxidation of silicon) which permits the initial patterning to be done when there is no surface topography to interfere with the uniform and continuous coating of the photoresist, unlike the LOCOS process which is done immediately prior to metallization. Delayed LOCOS is presented in claim 6. These claims are cancelled in this application.

A combination of all three techniques is used in fabricating an LC/ESI device, as presented in claims 10-12. These claims are cancelled in this application.

The combination of all three techniques, i.e., SMILE, Latent Masking, and Delayed LOCOS, but not specifically applied to making an LC/ESI device, is presented in claims 7-9. These claims are cancelled in this application.

A combination of SMILE and Delayed Locos is used in fabricating an ESI device, as presented in claims 14-16. A combination of SMILE and Delayed Locos, but not specifically applied to making an ESI device, is presented in claim 13. These claims are cancelled in this application.

A combination of Latent Masking and Delayed LOCOS is used in

fabricating an LC device, as presented in claims 20-22 and new claims 24-29. These claims are the subject of the present divisional application.

A combination of Latent Masking and Delayed LOCOS, but not specifically applied to making an LC device, is presented in claims 17-19. These claims are cancelled in this application.

A combination of SMILE and Latent Masking is presented in claim 23. This claim is cancelled in this application.

Thus, the independent claims cover three techniques and combinations thereof, as well as three devices made with three of the combinations of techniques. Perhaps it would be useful to recapitulate the claims and their techniques in claim sequence.

Claims 1-3: Latent Masking

Claim 4: SMILE (2 patterns)

Claim 5: SMILE (3 patterns)

Claim 6: Delayed LOCOS

Claims 7-9: SMILE plus Latent Masking plus Delayed LOCOS

Claims 10-12: SMILE plus Latent Masking plus Delayed LOCOS as applied to making an integrated LC/ESI device

Claim 13: SMILE plus Delayed LOCOS

Claims 14-16: SMILE plus Delayed LOCOS as applied to making an ESI device

Claims 17-19: Latent Masking plus Delayed LOCOS

Claims 20-22 and 24-29: Latent Masking plus Delayed LOCOS as applied to making an LC device

Claim 23: SMILE plus Latent Masking

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

If the Examiner believes that contact with Applicant's attorney would be advantageous toward the disposition of this case, the Examiner is herein requested to call Applicant's attorney at the telephone number noted below.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0289.

Respectfully submitted,

WALL MARJAMA & BILINSKI, LLP

Dated: 11/2/01 By: ______________________

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PATENT TRADEMARK OFFICE

"VERSION WITH MARKINGS TO SHOW CHANGES MADE."

In the Claims:

20. (Amended) A method for fabricating a liquid chromatography microelectromechanical device, comprising the steps of:

a) providing a silicon substrate having an introduction surface on an introduction side of said substrate and an opposing separation surface on a separation side of said substrate;

b) forming first and second silicon oxide layers on said introduction and separation surfaces of said substrate, respectively;

c) doping a portion of said introduction surface through said first silicon oxide layer with a dopant of a same conductivity type as a conductivity type of said substrate;

d) forming a silicon nitride film on said first silicon oxide layer;

e) patterning and etching said silicon nitride film to form at least one silicon nitride contact area on said first silicon oxide layer;

f) oxidizing said substrate, after step (e), to increase said first and second silicon oxide layers;

g) coating a first photoresist layer on said introduction side;

h) defining a first pattern on said first photoresist layer, said first pattern consisting of an introduction channel and an introduction-side exit channel;

i) transferring said first pattern onto said first silicon oxide layer;

j) etching said first pattern into said silicon substrate;

k) removing said first photoresist layer;

l) coating a second photoresist layer on said separation side;

m) defining and transferring a second pattern onto said second silicon oxide layer, said second pattern including a separation channel, a separation channel terminus, and a plurality of separation posts;

n) removing said second photoresist layer;

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substantially aligned with said introduction-side exit channel; otherwise, defining said third pattern onto said separation surface when said fluid reservoir is also included in said second pattern, such that said reservoir is substantially aligned with said introduction channel and said separation-side exit channel is substantially aligned with said introduction-side exit channel;

q) etching said third pattern into said silicon substrate so that said reservoir connects with said introduction channel and said separation-side exit channel connects with said introduction-side exit channel;

r) removing said third photoresist layer;

s) etching said second pattern into said silicon substrate;

t) forming, after step (s), an isolation layer on all silicon surfaces of said silicon substrate;

u) attaching, after step (t), a cover substrate to said separation surface of said silicon substrate;

v) removing, after step (u), said silicon nitride from said at least one silicon nitride contact area and removing any of said first silicon oxide layer beneath said at least one silicon nitride contact area, thereby forming at least one contact area on said first surface; and

w) depositing a metal on said at least one contact area.